The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte OSMAN KENT

Appeal No. 2006-1687
Application No. 10/086,980

HEARD: September 12, 2006

Before HAIRSTON, JERRY SMITH, and MACDONALD, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

This is an appeal from the final rejection of claims 1, 3 through 5 and 7 through 35.

The disclosed invention relates to a method and system for bypassing a defective one of a plurality of parallel graphics computational units, and distributing incoming tasks only among operative ones of the parallel graphics computational units.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A graphics processor, comprising:

   a plurality of parallellized graphics computational units; and

   one or more task allocation units programmed to bypass defective ones of said units within said groups, and to distribute incoming tasks only among operative ones of said units .

The references relied on by the examiner are:

Brent et al. (Brent)	5,459,864	Oct. 17, 1995
Baldwin	6,025,853	Feb. 15, 2000

Claims 1, 3 through 5 and 7 through 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baldwin in view of Brent.

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 3 through 5 and 7 through 35.

We agree with the examiner's finding (answer, page 3) that "Baldwin teaches a graphics processor [Figure] (2E) comprising a plurality of parallelized graphics computational units (col. 64, lines 16-21, 25-29 and 38-40), such as, rasterizer, scissor, stipple, alpha test, fog, texture, stencil test, depth test, local and frame buffer controllers." We additionally agree with the examiner's finding (answer, page 3) that "Baldwin fails to explicitly teach or suggest one or more task allocation units programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits."

With respect to Brent, we agree with the examiner's finding (answer, page 3) that "Brent teaches a load balancing, error recovery and reconfiguration control in a data movement subsystem with cooperating plural queue processors (Fig. 2, abstract, col. 2, lines 39-45, col. 5,

lines 49-52 and col. 6, lines 11-18)." We do not, however, agree with the examiner's conclusion (answer, pages 3 and 4) that it would have been obvious to the skilled artisan to modify the teachings of Baldwin with the teachings of Brent for the advantage of "automatic load balancing among plural processors, automatic recovery from any failing processor, and automatic reconfiguration for the subsystem containing the processors without intervention from the operating system as taught by Brent (col. 1, lines 18-24)" because Baldwin only uses a single graphics processor. If Baldwin's single graphics processor fails, then the system will cease to function for lack of another graphics processor to turn to for help (brief, page 15).

In summary, the rejection of claims 1, 3 through 5 and 7 through 35 is reversed for lack of a prima facie case of obviousness.

DECISION

The decision of the examiner rejecting claims 1, 3 through 5 and 7 through 35 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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JERRY SMITH) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
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